

FEATURES **IEEE802.3af Compatible**

- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 10 μ A (Max.) @ $V_{DS} = 100V$
- Lower $R_{DS(ON)}$: 0.155 Ω (Typ.)

$BV_{DSS} = 100 V$
 $R_{DS(on)} = 0.2 \Omega$
 $I_D = 2.3 A$

SOT-223



1. Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	100	V
I_D	Continuous Drain Current ($T_A=25^\circ C$)	2.3	A
	Continuous Drain Current ($T_A=70^\circ C$)	1.84	
I_{DM}	Drain Current-Pulsed ^①	18	A
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulsed Avalanche Energy ^②	123	mJ
I_{AR}	Avalanche Current ^①	2.3	A
E_{AR}	Repetitive Avalanche Energy ^①	0.24	mJ
dv/dt	Peak Diode Recovery dv/dt ^③	6.5	V/ns
P_D	Total Power Dissipation ($T_A=25^\circ C$) *	2.4	W
	Linear Derating Factor *	0.019	W/ $^\circ C$
T_J, T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	$^\circ C$
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient *	--	52	$^\circ C/W$

* When mounted on the minimum pad size recommended (PCB Mount).

Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	100	--	--	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	0.12	--	V/ $^\circ\text{C}$	$I_D=250\mu A$ See Fig 7
$V_{GS(th)}$	Gate Threshold Voltage	2.0	--	4.0	V	$V_{DS}=5V, I_D=250\mu A$
I_{GSS}	Gate-Source Leakage, Forward	--	--	100	nA	$V_{GS}=20V$
	Gate-Source Leakage, Reverse	--	--	-100		$V_{GS}=-20V$
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	μA	$V_{DS}=30V$ ⑥
		--	--	10		$V_{DS}=100V$
		--	--	100		$V_{DS}=80V, T_A=125^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	0.2	Ω	$V_{GS}=10V, I_D=1.15A$ ④
g_{fs}	Forward Transconductance	--	3.12	--	S	$V_{DS}=40V, I_D=1.15A$ ④
C_{iss}	Input Capacitance	--	370	480	pF	$V_{GS}=0V, V_{DS}=25V, f=1\text{MHz}$ See Fig 5
C_{oss}	Output Capacitance	--	95	110		
C_{rss}	Reverse Transfer Capacitance	--	38	45		
$t_{d(on)}$	Turn-On Delay Time	--	14	40	ns	$V_{DD}=50V, I_D=9.2A,$ $R_G=18\Omega$ See Fig 13 ④ ⑤
t_r	Rise Time	--	14	40		
$t_{d(off)}$	Turn-Off Delay Time	--	36	90		
t_f	Fall Time	--	28	70		
Q_g	Total Gate Charge	--	16	22	nC	$V_{DS}=80V, V_{GS}=10V,$ $I_D=9.2A$ See Fig 6 & Fig 12 ④ ⑤
Q_{gs}	Gate-Source Charge	--	2.7	--		
Q_{gd}	Gate-Drain("Miller") Charge	--	7.8	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I_S	Continuous Source Current	--	--	2.3	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current ①	--	--	18		
V_{SD}	Diode Forward Voltage ④	--	--	1.5	V	$T_J=25^\circ\text{C}, I_S=2.3A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	--	98	--	ns	$T_J=25^\circ\text{C}, I_F=9.2A$
Q_{rr}	Reverse Recovery Charge	--	0.34	--	μC	$di_F/dt=100A/\mu s$ ④

Notes ;

- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- ② $L=35\text{mH}, I_{AS}=2.3A, V_{DD}=25V, R_G=27\Omega,$ Starting $T_J=25^\circ\text{C}$
- ③ $I_{SD}\leq 9.2A, di/dt\leq 300A/\mu s, V_{DD}\leq BV_{DSS},$ Starting $T_J=25^\circ\text{C}$
- ④ Pulse Test : Pulse Width = $250\mu s,$ Duty Cycle $\leq 2\%$
- ⑤ Essentially Independent of Operating Temperature
- ⑥ Adjusted for Cisco

Fig 1. Output Characteristics

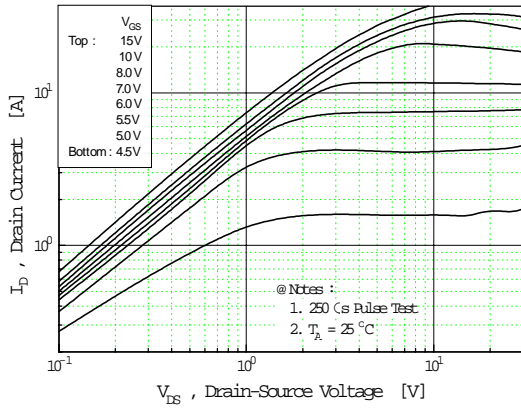


Fig 2. Transfer Characteristics

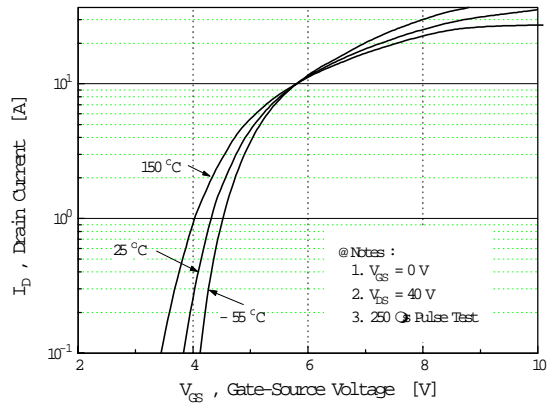


Fig 3. On-Resistance vs. Drain Current

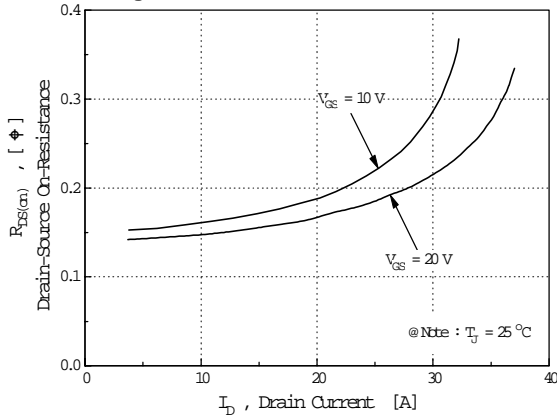


Fig 4. Source-Drain Diode Forward Voltage

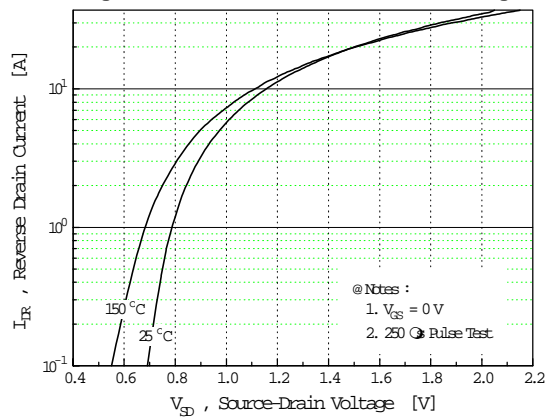


Fig 5. Capacitance vs. Drain-Source Voltage

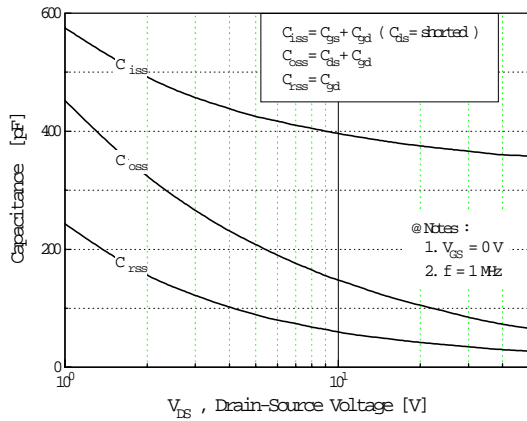


Fig 6. Gate Charge vs. Gate-Source Voltage

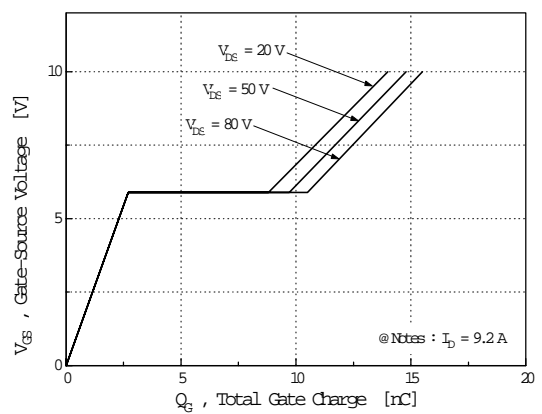


Fig 7. Breakdown Voltage vs. Temperature

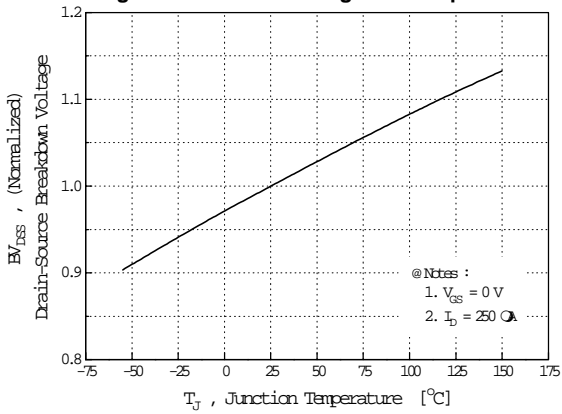


Fig 8. On-Resistance vs. Temperature

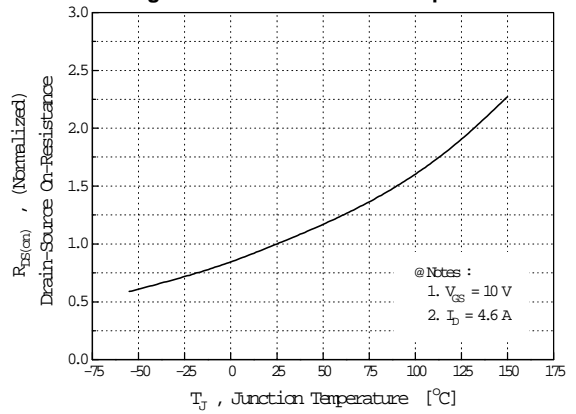


Fig 9. Max. Safe Operating Area

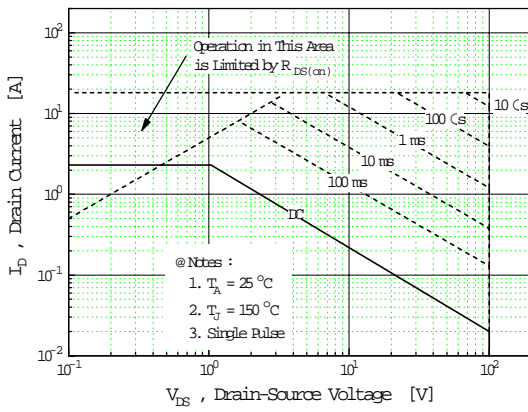


Fig 10. Max. Drain Current vs. Ambient Temperature

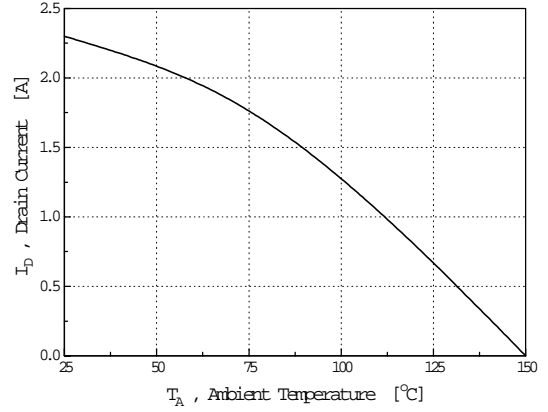


Fig 11. Thermal Response

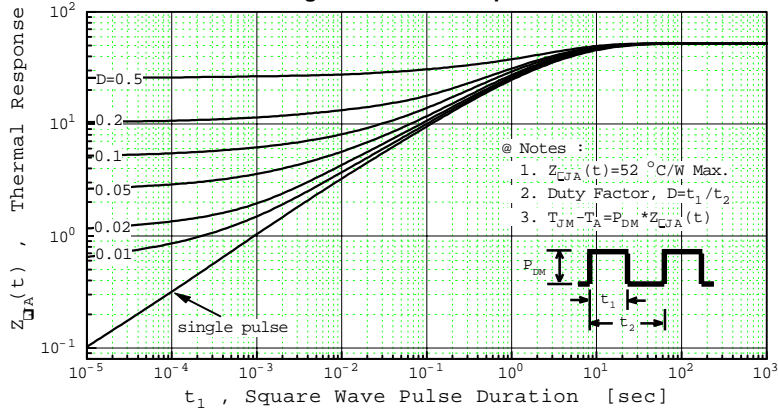


Fig 12. Gate Charge Test Circuit & Waveform

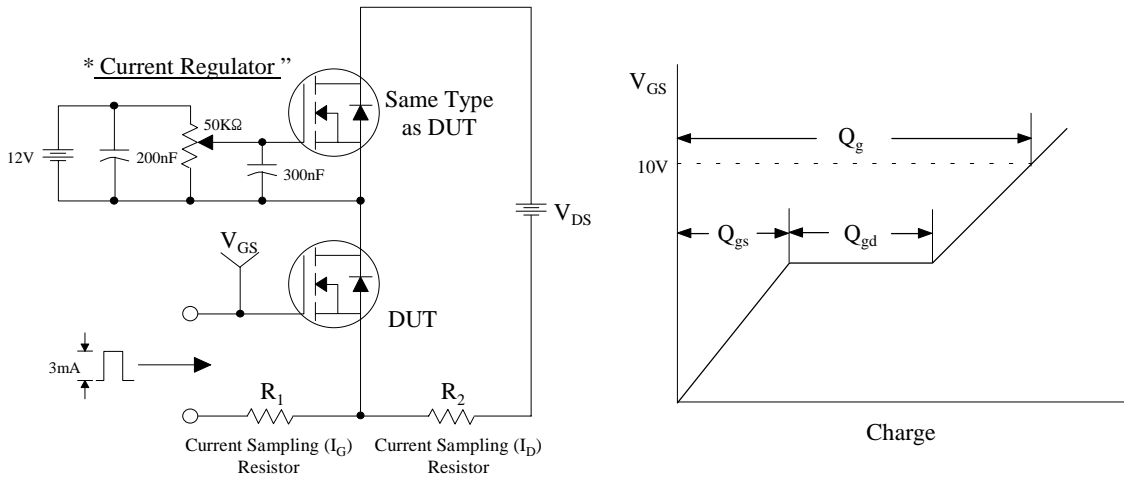


Fig 13. Resistive Switching Test Circuit & Waveforms

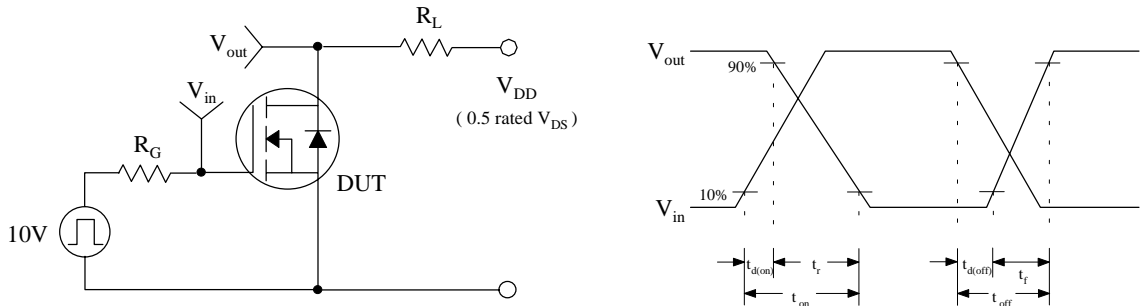


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

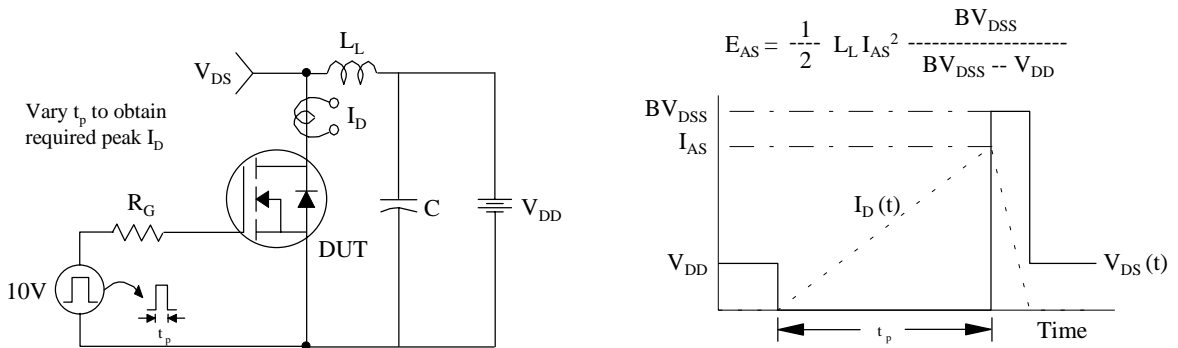
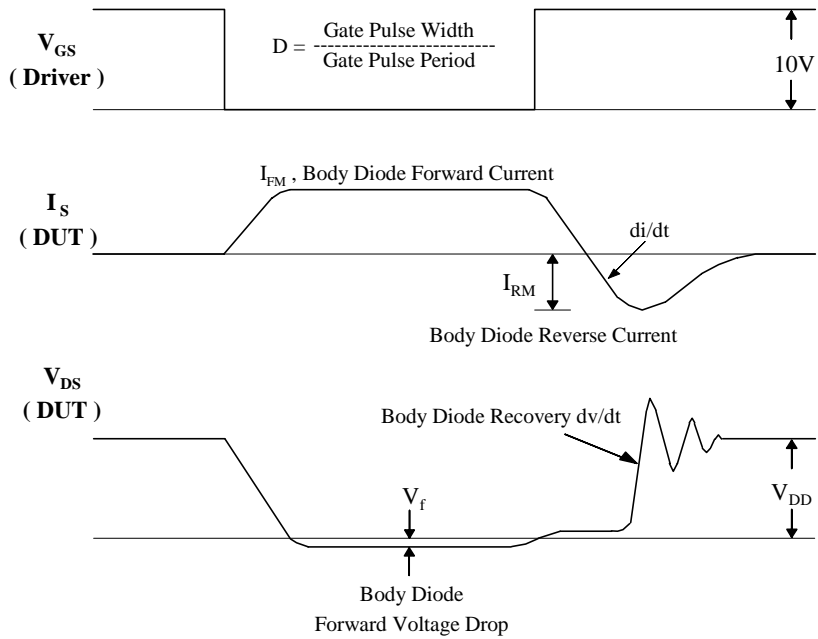
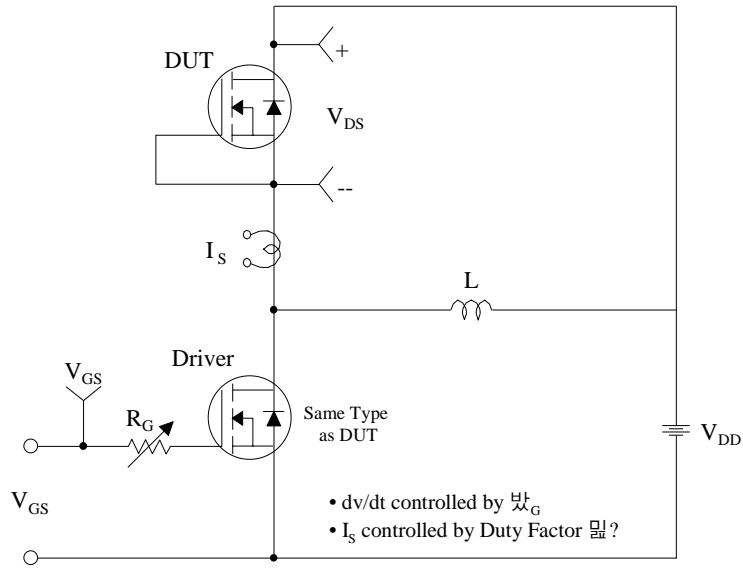


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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